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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/654,226

09/02/2003

Ammar Derraa

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06/15/2004

TRASK BRITT

P.O. BOX 2550

SALT LAKE CITY, UT 84110

EXAMINER

SANTIAGO, MARICELI

ART UNIT

PAPER NUMBER

2879

DATE MAILED: 06/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/654,226	DERRAA, AMMAR	
	Examiner	Art Unit	
	Mariceli Santiago	2879	<i>pm</i>

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION***Response to Amendment***

The Amendment, filed on March 4, 2004, has been entered and acknowledged by the Examiner.

Claims 1-18 are pending in the instant application.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-18 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 10 and 14 of U.S. Patent No. 6,326,222. Although the conflicting claims are not identical, they are not patentably distinct from each other for the following reasons.

U.S. Application SN 10/654,226	U.S. Patent No. 6,326,222	Reasons for rejection under obviousness-type double patenting
Claim 1	Claim 1	Patent '222 claims a method of fabricating at least one emission structure, comprising forming at least one conductive structure extending across at least a portion of a substrate, substantially removing a longitudinal portion of the at least one conductive structure (patterning) to define at least one conductive layer substantially perpendicular (parallel rows) to the substrate, the

		substrate being exposed along a length of the at least one conductive layer, and forming at least one emission structure adjacent the at least one conductive layer.
Claim 2	Claim 1	Patent '222 claims a method wherein the at least one emission structure includes an emitter tip.
Claim 3	Claim 1	Patent '222 claims a method wherein the at least one emission structure includes a corresponding resistor.
Claim 4	Claim 1	Patent '222 claims a method wherein the resistor is adjacent the at least one conductive layer.
Claim 5	Claim 1	Patent '222 claims a method wherein the at least one emission structure comprises a plurality of lines of emission structures.
Claim 6	Claim 1	Patent '222 claims a method wherein the emission structure located along a first line of the plurality of lines is isolated from at least one emission structure located an adjacent, second line of the plurality of lines.
Claim 7	Claim 1	Patent '222 claims a method wherein the conductive material over the substrate is patterned.
Claim 8	Claim 1	Patent '222 claims a method wherein the at least one emission structure is formed from at least one of semiconductive or conductive materials.
Claim 9	Claim 10	Patent '222 claims a method wherein the at least one emission structure extends over a lateral (peripheral) edge of the at least one conductive structure.
Claim 10	Claim 1	Patent '222 claims a method for fabricating at least one emission structure, comprising forming at least one conductive structure that extends at least partially across a substrate, forming at least one emitter tip and a corresponding resistor adjacent to the at least one conductive structure, and substantially removing (patterning) at least a longitudinal portion of the at least one conductive structure along substantially an entire length thereof to define at least one conductive layer substantially perpendicular (parallel rows) to the substrate.
Claim 11	Claim 1	Patent '222 claims a method wherein the conductive material over the substrate is patterned.

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Claim 12	Claim 1	Patent '222 claims a method wherein the at least one emission structure is formed from at least one of semiconductive or conductive materials.
Claim 13	Claim 1	Patent '222 claims a method wherein the at least one emission/resistor structure is formed from at least one of semiconductive or conductive materials.
Claim 14	Claim 14	Patent '222 claims a method wherein forming the at least one emitter tip comprises disposing at least one layer comprising at least one of semiconductive material and conductive material over the substrate and the at least one conductive structure, removing a longitudinal portion of at least one region of the at least one layer located over the at least one conductive structure to expose at least a substantially longitudinal portion of the at least one conductive structure, and patterning at least one remaining portion of the at least one layer.
Claim 15	Claim 14	Patent '222 claims a method wherein at least one emitter tip is defined.
Claim 16	Claim 14	Patent '222 claims a method including a corresponding resistor.
Claim 17	Claim 10	Patent '222 claims a method wherein the substantially removing comprises leaving at least a lateral edge (conductive traces) of the at least one conductive structure along substantially the entire length thereof
Claim 18	Claim 10	Patent '222 claims a method wherein the at least one emission structure extends over a lateral (peripheral) edge of the at least one conductive structure.

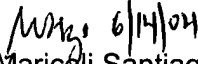
Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mariceli Santiago whose telephone number is (571) 272-2464. The examiner can normally be reached on Monday-Friday from 9:30 AM to 6:00 PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel, can be reached on (571) 272-2457. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Mariceli Santiago
Patent Examiner
Art Unit 2879